10/648223

SD

09/16/04

CLAIM 1 CANCELLED

Claim 2 (Currently Amended) A semiconductor device comprising:

a plurality of gate electrode structures formed on a semiconductor substrate, each of which comprises:

a gate insulating film formed on said semiconductor substrate;

a gate electrode formed on said gate insulating film; and

an offset spacer formed on a side face of said gate electrode,

wherein respective lengths of said plurality of gate electrode structures are substantially uniform with one another, each of said lengths being defined as a sum of a gate length extending on an interface between said gate insulating film and said gate electrode, and a width of said offset spacer extending on an interface between said offset spacer and said semiconductor substrate, and

~~wherein~~ said plurality of gate electrode structures ~~includes~~ include a first gate electrode having a rectangular section, ~~an~~ a second gate electrode having a upwardly tapered ~~gate electrode~~ section, and a third gate electrode having a downwardly tapered section, ~~gate electrode which are provided on the same semiconductor substrate.~~

Claim 3 (Currently Amended) The semiconductor device according to claim [[3]] 2,

wherein a pair of shallow source/drain regions and a pair of deep source/drain regions are formed to form a MOSFET, said regions in each of said pairs being formed in said semiconductor substrate on opposite sides of a portion of said semiconductor substrate immediately under said gate electrode.

CLAIMS 4 THROUGH 6 ARE CANCELLED